WHAT IS CLAIMED IS:

1. A liquid crystal display having a normal drive period when liquid crystals are normally driven after alignment of the liquid crystals injected between upper/lower plates is changed from a splay state to a bend state at a voltage higher than a transition voltage, comprising:

a liquid crystal display panel having a thin film transistor at each intersection part of a plurality of data lines and a plurality of gate lines;

a gate driver configured to supply a gate high voltage and a gate low voltage during a data input period, and sequentially supply a gate reset voltage to gate lines during a reset period, wherein the normal drive period is divided into the data input period and the reset period;

a data driver configured to supply data voltages to the data lines in accordance with gate voltages applied to the gate lines; and

a timing controller configured to control the data voltages supplied to the data lines and the gate voltages supplied to the gate lines.

2. The liquid crystal display according to claim 1, wherein the gate driver is configured to supply the gate high voltage to the gate lines during an on-period for the thin film transistor in the data input period, and to supply the gate low voltage to the gate lines during an off-period for the thin film transistor.

3. The liquid crystal display according to claim 1, wherein the gate reset voltage is a designated voltage set to be lower than the gate low voltage.

4. The liquid crystal display according to claim 1, wherein the gate reset voltage and the gate low voltage, which are alternately applied to a previous gate line, constitute an AC voltage.

5. The liquid crystal display according to claim 4, wherein a half period of the AC voltage is set to be less than a response time of the liquid crystals.

6. The liquid crystal display according to claim 4, wherein the gate low voltage applied for the data input period is the same as an average value of the AC voltage.

7. The liquid crystal display according to claim 1, wherein the gate high voltage is applied at least two times for the data input period.

8. The liquid crystal display according to claim 1, wherein the gate reset voltage is an AC voltage having positive and negative polarities alternated on the basis of the gate low voltage for each frame.

9. The liquid crystal display according to claim 1, wherein the gate reset voltage is an AC voltage.

10. A driving method of a liquid crystal display having a normal drive period when liquid crystals are normally driven after alignment of the liquid crystals injected between upper/lower plates is changed from a splay state to a bend state at a voltage higher than a transition voltage, comprising:

forming a thin film transistor at each intersection part of a plurality of data lines and a plurality of gate lines;

dividing the normal drive period into a data input period and a reset period;

supplying a gate high voltage and a gate low voltage to the gate lines for the data input period;

supplying a gate reset voltage sequentially to the gate lines to make an average voltage of liquid crystal cells higher than the transition voltage for the reset period; and

supplying a data reset voltage to the data lines in accordance with the gate reset voltage.

11. The liquid crystal display according to claim 10, wherein supplying the gate high and gate low voltages includes supplying the gate high voltage to the gate lines during an

on-period for the thin film transistor, and supplying the gate low voltage to the gate lines during an off-period for the thin film transistor.

12. The liquid crystal display according to claim 10, wherein the gate reset voltage is a designated voltage set to be lower than the gate low voltage.

13. The liquid crystal display according to claim 10, wherein the gate reset voltage and the gate low voltage, which are alternated, constitute an AC voltage.

14. The liquid crystal display according to claim 13, wherein a half period of the AC voltage is set to be less than a response time of the liquid crystals.

15. The liquid crystal display according to claim 10, wherein the gate low voltage applied for the data input period is the same as an average value of the AC voltage.

16. The liquid crystal display according to claim 13, wherein the gate high voltage is applied at least two times for the data input period.

17. The liquid crystal display according to claim 10, wherein the gate reset voltage is an AC voltage having positive and negative polarities alternated on the basis of the gate low voltage for each frame.

18. The liquid crystal display according to claim 1, wherein the gate reset voltage is an AC voltage.